

REMARKS

The Office action mailed on 22 April 2004 (Paper No. 8) has been carefully considered.

The specification is being amended to correct minor errors and improve form. Claims 9, 10, 14, 18 and 33 are being cancelled without prejudice or disclaimer, and claims 1, 4, 11 thru 13, 15 thru 17, 19, 20, 25, 26, 28 and 34 thru 40 are being amended. Thus, claims 1 thru 8, 11 thru 13, 15 thru 17, 19 thru 32 and 34 thru 40 are pending in the application.

It should be noted that the amendments to the specification are being made merely for the purpose of improving form or correcting minor errors. Thus, no "new matter" is being introduced into the specification, and no new issues requiring further consideration and/or search are being raised.

It should also be noted that the claims are being amended for the purpose of improving their form, or to combine independent and dependent claims so as to distinguish the invention from the prior art cited by the Examiner. Thus, the amendments to the claims do not raise new issues requiring further consideration and/or search by the Examiner, and therefore this Amendment After Final should be entered.

In paragraph 2 of the Office action, the Examiner rejected claims 1 thru 13, 16 thru 25, 27 thru 33, 36, 37 and 40 under 35 U.S.C. §102 for alleged anticipation by Mokhtari *et al.*, entitled *BIT-RATE TRANSPARENT ELECTRONIC DATA REGENERATION IN REPEATERS FOR HIGH SPEED LIGHTWAVE COMMUNICATION SYSTEMS*, Proceedings of the 1999 IEEE, International Symposium, Vol. 2, pp. 508-511. In paragraph 4 of the Office action, the Examiner rejected claims 15, 26 and 35 under 35 U.S.C. §103 for alleged unpatentability over Mokhtari *et al.* in view of Uda *et al.*, European Patent Publication No. 0342010. In paragraph 5 of the Office action, the Examiner rejected claims 14, 34 and 38 under 35 U.S.C. §103 for alleged unpatentability over Mokhtari *et al.* in view of Ishihara, U.S. Patent No. 5,557,648. In paragraph 6 of the Office action, the Examiner rejected claims 39 and 40 under 35 U.S.C. §103 for alleged unpatentability over Mokhtari *et al.* in view of Ishihara '648, and further in view of Uda *et al.* '010. For the reasons stated below, it is submitted that the invention recited in the claims, as now amended, is distinguishable from the prior art cited by the Examiner so as to preclude rejection under 35 U.S.C. §102 or §103.

The present invention generally relates to a method and apparatus for measuring the bit-rate of a received signal in a wavelength division multiplexing (WDM) transfer mode. The method include the steps of: duplicating the received signal to output two signals as a received signal; delaying one of the signals by a predetermined time; and performing an exclusive OR logical operation on the delayed signal and the other signal

which is not delayed to generate a sensing signal. The sensing signal is then low-pass filtered and converted to digital form, and the direct current voltage of the filtered and digitized sending signal is measured to derive the bit-rate of the received signal. The derived bit rate is then used by a reference clock generator to generate a reference clock signal which is applied to a programmable recovery circuit, and the latter recovers the data and clock signal. Accordingly, when various signals having different bit-rates are used over a network in the WDM system, a receiving terminal can automatically recognize information under a bit-rate of a received optical signal and extract a reference clock signal from the received signal, thereby reproducing the received optical signal without distortion, using the clock signal.

The primary reference cited against the claims of this application is Mokhtari *et al.*, entitled *BIT-RATE TRANSPARENT ELECTRONIC DATA REGENERATION IN REPEATERS FOR HIGH SPEED LIGHTWAVE COMMUNICATION SYSTEMS*, Proceedings of the 1999 IEEE, International Symposium, Vol. 2, pp. 508-511. The Mokhtari *et al.* reference relates to two approaches for realization of bit-rate transparent data regeneration: 1) locked oscillator, phase-locking structures (partially bitrate transparent); 2) freerunning (unlocked) oscillator, sampling structures (fully bitrate transparent).

In Mokhtari *et al.*, a 3R repeater (as shown in Figure 1) includes a Reamp. stage, a

reshaping stage, a limit stage, a retimer, and a driver. The Reamp. stage includes an optical/electrical converter and an amplifier for converting and amplifying the original signal, whereupon the converted and amplified signal is then reshaped, limited, and retimed, with the resultant signal being provided to the driver. As further disclosed, the retimer stage generally includes a clock and a decision circuit as shown in Figure 2 of Mokhtari *et al.*. One arrangement for clock recovery, based on phased locked loop, is shown in Figure 3 of Mokhtari *et al.*, and includes an edge detector, a phase locked loop (PLL), a delay circuit and a decision circuit. The decision circuit is shown in more detail in Figure 4, while the edge detector is shown in more detail in Figure 5.

The secondary references cited by the Examiner are Uda *et al.*, European Patent Publication No. 0342010, and Ishihara, U.S. Patent No. 5,557,648. Uda '010 relates to a digital signal regenerator which can produce a regenerated data pulse stream with reduced decision errors, permits the use of a phase adjustable clock pulse sequence with no deterioration in rise and fall characteristics of recovered clock pulses, and is adaptable to a high bit rate data pulse stream. Ishihara '648 relates to a phase lock loop circuit that can be formed into a full monolithic integrated circuit without an external component part, and that can maintain the phase locked state even for a consecutive identical bit state of input data including more than several tens of consecutive identical bits.

The present invention differs from the arrangement of Mokhtari *et al.* in several

respects. First, in the invention, a first unit 40a (see Figure 3 of the application) of the identification unit 50 (see Figure 2) delays the original electrical signal provided by the O/E converter 10 and amplifier 20. In contrast, in Mokhtari *et al.*, the original electrical signal provided by the O/E converter and amplified in the Reamp. stage of Figure 1 is processed by a reshaping circuit and a limit stage, and a resultant reshaped and limited signal is provided to the retimer of Figure 1 wherein delaying takes place.

Second, whereas the Examiner has argued that the edge detector of Figures 3 and 5 of Mokhtari *et al.* performs functions (delaying, exclusive-OR, *etc.*) of the first unit of the identification unit (recited in claim 1), and whereas the Examiner has further argued that the PLL of Figure 3 of Mokhtari *et al.* performs the functions (filtering and bit rate detection) of the second unit of the identification unit recited in claim 1, and whereas the Examiner is apparently further arguing that the delay circuit of Figure 3 of Mokhtari *et al.* performs the function (generating a reference clock signal in dependence upon the detected bit rate) of the clock generator as recited in claim 1, it does not appear that Mokhtari *et al.* discloses a recovery unit recovering an input clock signal and data from the input optical signal in dependence upon the reference clock signal, as recited in claim 1. In fact, in Figure 3 of Mokhtari *et al.*, the decision circuit receives the clock output of the delay circuit, and then generates a recovered data output, whereas the clock output of Figure 3 is generated by the delay circuit itself, and not by the decision circuit.

By way of further distinguishing the invention from the prior art cited by the Examiner, it is noted that Mokhtari *et al.* discloses a configuration in which a clock is extracted from an input optical signal (*see* Figures 3 and 5 of the reference). It is also noted that, although the term “retime” or “retiming” might appear in Mokhtari *et al.*, it has a different meaning from the meaning of “retiming” as disclosed in the present application.

In addition, in the present invention, after recognizing the bit-rate of an input signal, an accurate reference clock is generated from a separate reference clock generator or separately. In contrast, in Mokhtari *et al.*, the clock signal is extracted from the input signal directly (again, *see* Figures 3 and 5 of the reference). This is technology used in a so-called “protocol fee system”, which is mentioned as prior art in the present application. Such technology, as employed in Mokhtari *et al.*, has a problem typical of the prior art (as discussed in the “Related Art” section of the application) in that noise and timing jitter accumulate and increase by passing through a node with resultant decrease in transmission quality (*see* page 9, line 16 - page 10, line 4 of the specification of the present application).

Furthermore, the present invention is distinguishable from the prior art due to the fact that the present invention is characterized in that an original signal and a delay signal are subjected to an exclusive-OR operation, and the resultant signal is then low-pass

filtered prior to being converted into digital form (*see* Figure 3 of the present application and the related discussion in the specification thereof). Once the latter operations are performed in accordance with the present invention, a bit rate is derived according to a voltage level of the output signal emanating from the digital converter (again, *see* Figure 3 and the related discussion in the specification of the present application).

In contrast, in Mokhtari *et al.*, a low-pass filter is disclosed, but it is not used for the same type of operation as in the present invention. Furthermore, Mokhtari *et al.* fails to disclose or suggest use of the voltage level of the resultant signal, as well as reorganization of the bit rate according to the voltage level, the latter two operations being at the heart of the present invention.

Turning to consideration of the claims, independent claim 1 is being amended to include the recitations from dependent claim 14, which is being cancelled. Thus, independent claim 1 recites the invention in a manner distinguishable from the prior art by virtue of the fact that the prior art does not disclose or suggest an identification unit which comprises first and second units with the respective functions recited in the claim, including the performance of an exclusive-OR operation upon first and second signals in the first unit so as to form a third signal, and filtering the third signal so as to detect a bit rate in dependence upon a voltage level of the filtered third signal. Moreover, the prior art does not disclose or suggest a second unit which comprises a filter for filtering the

third signal in combination with the analog-to-digital converter for converting the filtered third signal from the analog to digital form, as well as a bit rate deriving unit for deriving a bit rate in dependence upon information related to voltage level of the digital signal and a predetermined bit rate, as now recited in amended claim 1.

Independent method claim 17 is being amended in such a manner as to distinguish the inventive method from the prior art cited by the Examiner. Thus, the prior art cited by the Examiner does not disclose or suggest the generation of a “resultant signal” by performing an exclusive-OR operation on a first signal and a second signal corresponding to an original signal delayed by a predetermined quantity of time and an original signal not delayed, respectively, and the prior art does not disclose or suggest the determination of a bit rate of the original signal by low-pass filtering the resultant signal, and by determining a voltage level of the low-pass filtered resultant signal. Finally, the prior art does not disclose or suggest the step of generating a reference clock signal separate from the original signal and in dependence upon the bit rate as determined in the previous step.

Independent apparatus claim 28 is being amended to include the recitations from dependent claim 33, which is being cancelled. Thus, independent claim 28 recites the apparatus as comprising the combination of a converter, an identification unit, a clock generator and a recovery unit, and claim 28 further recites the identification unit as

comprising a first unit and a second unit having the functions previously recited in dependent claim 33, and discussed above relative to independent claim 1. Thus, independent claim 28 recites the invention in a manner distinguishable from the prior art because the prior art does not disclose or suggest an identification unit comprising a first unit for delaying an original electrical signal, for performing an exclusive-OR operation upon a first signal corresponding to the original electrical signal delayed by predetermined quantity of time, and a second signal corresponding to the original electrical signal not delayed, the first unit forming a third signal as a result of the exclusive-OR operation. Moreover, the prior art does not disclose or suggest an identification unit which includes a second unit for filtering the third signal, and for detecting the bit rate of the original signal in dependence upon a voltage level of the filtered third signal.

In view of the above, it is submitted that the claims of this application are in condition for allowance, and early issuance thereof is solicited. Should any questions remain unresolved, the Examiner is requested to telephone Applicant's attorney.

A Request for Continued Examination and its appropriate fee accompany this Amendment. Should the check become lost, be deficient in payment, or should other fees be incurred, the Commissioner is authorized to charge Deposit Account No. 02-4943 of Applicant's undersigned attorney in the amount of such fees.

Respectfully submitted,



Robert E. Bushnell,
Attorney for the Applicant
Registration No.: 27,774

1522 "K" Street N.W., Suite 300
Washington, D.C. 20005
(202) 408-9040

Folio: P56077
Date: 7/22/04
I.D.: REB/JGS